

## VII. Digitization of Pulse Height – Analog to Digital Conversion

For data storage and subsequent analysis the analog signal at the shaper output must be digitized.

Important parameters for ADCs used in detector systems:

1. Resolution  
The “granularity” of the digitized output
2. Differential Non-Linearity  
How uniform are the digitization increments?
3. Integral Non-Linearity  
Is the digital output proportional to the analog input?
4. Conversion Time  
How much time is required to convert an analog signal to a digital output?
5. Count-Rate Performance  
How quickly can a new conversion commence after completion of a prior one without introducing deleterious artifacts?
6. Stability  
Do the conversion parameters change with time?

Instrumentation ADCs used in industrial data acquisition and control systems share most of these requirements. However, detector systems place greater emphasis on differential non-linearity and count-rate performance. The latter is important, as detector signals often occur randomly, in contrast to measurement systems where signals are sampled at regular intervals.

## 1. Resolution

Digitization incurs approximation, as a continuous signal distribution is transformed into a discrete set of values. To reduce the additional errors (noise) introduced by digitization, the discrete digital steps must correspond to a sufficiently small analog increment.

Simplistic assumption:

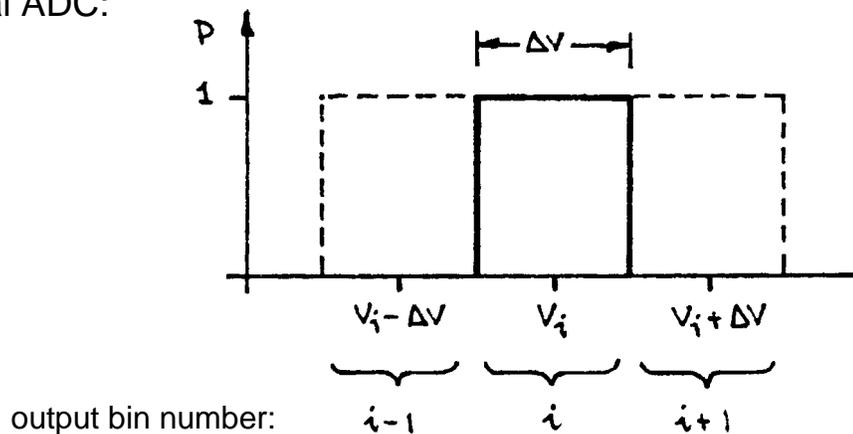
Resolution is defined by the number of output bits, e.g.

$$13 \text{ bits} \rightarrow \frac{\Delta V}{V} = \frac{1}{8192} = 1.2 \cdot 10^{-4}$$

### True Measure: Channel Profile

Plot probability vs. pulse amplitude that a pulse height corresponding to a specific output bin is actually converted to that address.

Ideal ADC:



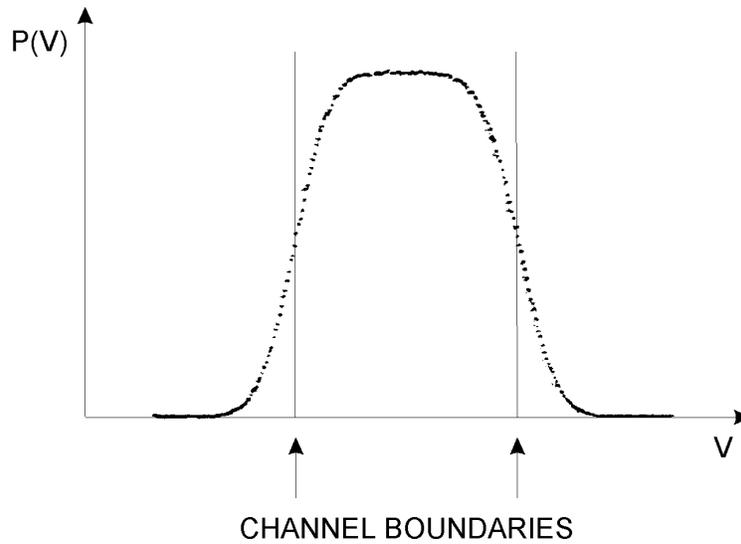
Measurement accuracy:

- If all counts of a peak fall in one bin, the resolution is  $\Delta V$ .
- If the counts are distributed over several (>4 or 5) bins, peak fitting can yield a resolution of  $10^{-1} - 10^{-2} \Delta V$ .

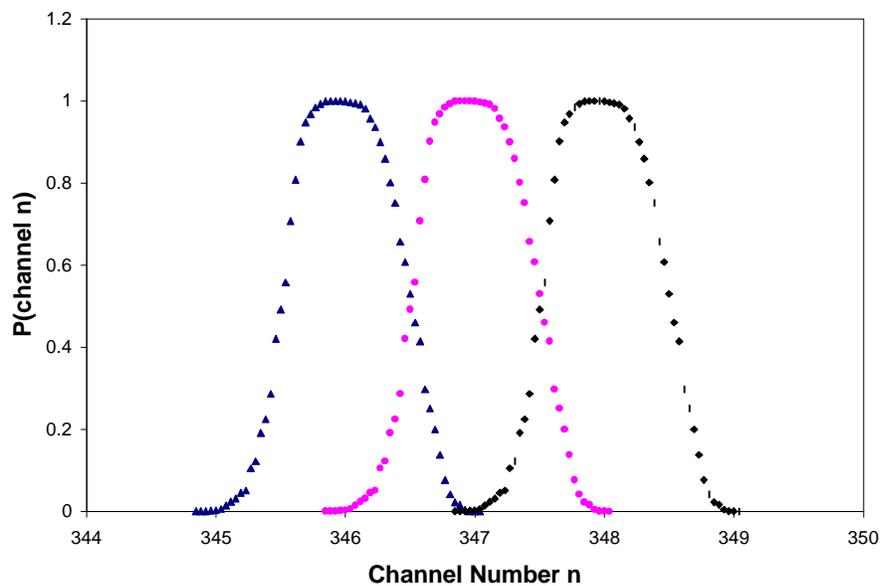
In reality, the channel profile is not rectangular as sketched above.

Electronic noise in the threshold discrimination process that determines the channel boundaries “smears” the transition from one bin to the next.

Measured channel profile (13 bit ADC)



The profiles of adjacent channels overlap



## 2. Differential Non-Linearity

Differential non-linearity is a measure of the inequality of channel profiles over the range of the ADC.

Depending on the nature of the distribution, either a peak or an rms specification may be appropriate.

$$DNL = \max \left\{ \frac{\Delta V(i)}{\langle \Delta V \rangle} - 1 \right\}$$

or

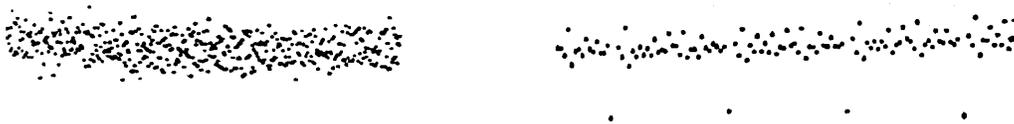
$$DNL = \text{r.m.s.} \left\{ \frac{\Delta V(i)}{\langle \Delta V \rangle} - 1 \right\}$$

where  $\langle \Delta V \rangle$  is the average channel width and  $\Delta V(i)$  is the width of an individual channel.

Differential non-linearity of  $< \pm 1\%$  max. is typical, but state-of-the-art ADCs can achieve  $10^{-3}$  rms, i.e. the variation is comparable to the statistical fluctuation for  $10^6$  random counts.

Note: Instrumentation ADCs are often specified with an accuracy of  $\pm 0.5$  LSB (least significant bit), so the differential non-linearity may be 50% or more.

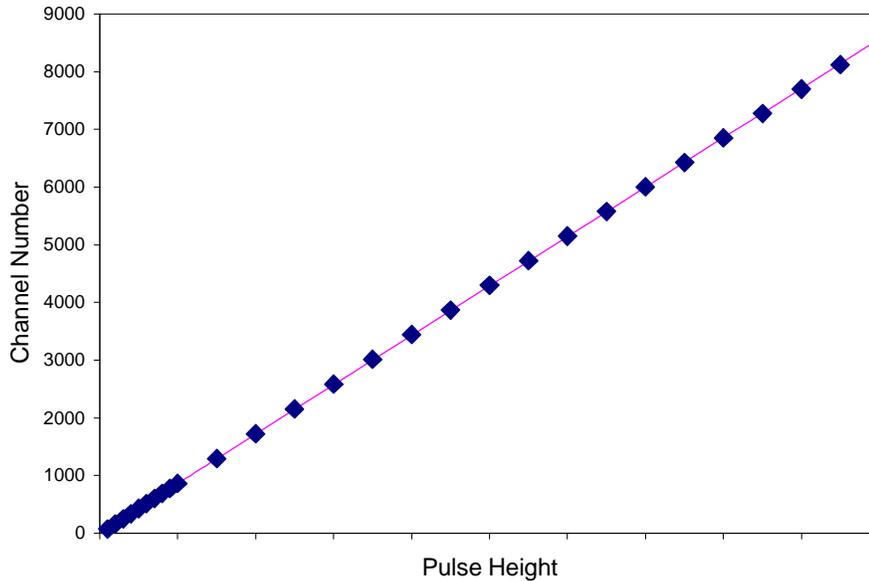
Typical differential non-linearity patterns (“white” input spectrum).  
An ideal ADC would show an equal number of counts in each bin.



The spectrum to the left shows a random pattern, but note the multiple periodicities visible in the right hand spectrum.

### 3. Integral Non-Linearity

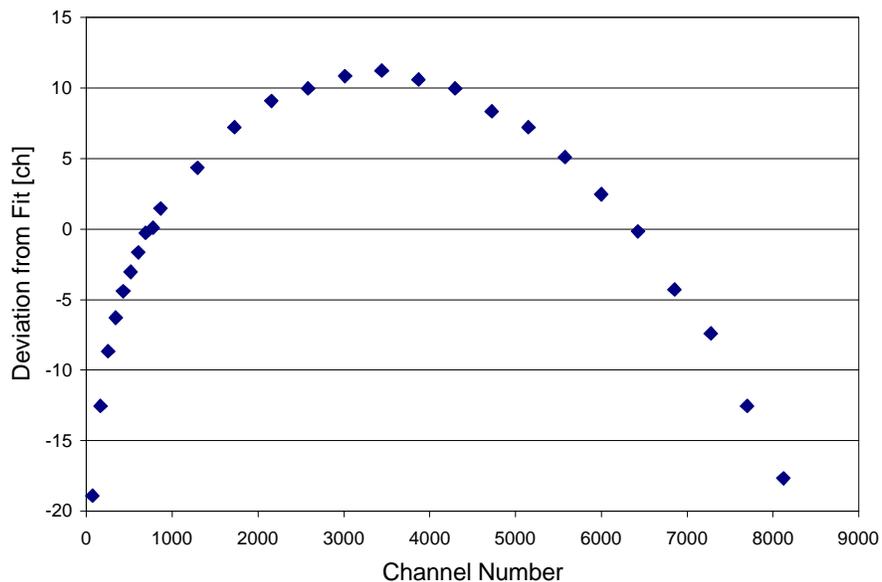
Integral non-linearity measures the deviation from proportionality of the measured amplitude to the input signal level.



The dots are measured values and the line is a fit to the data.

This plot is not very useful if the deviations from linearity are small.

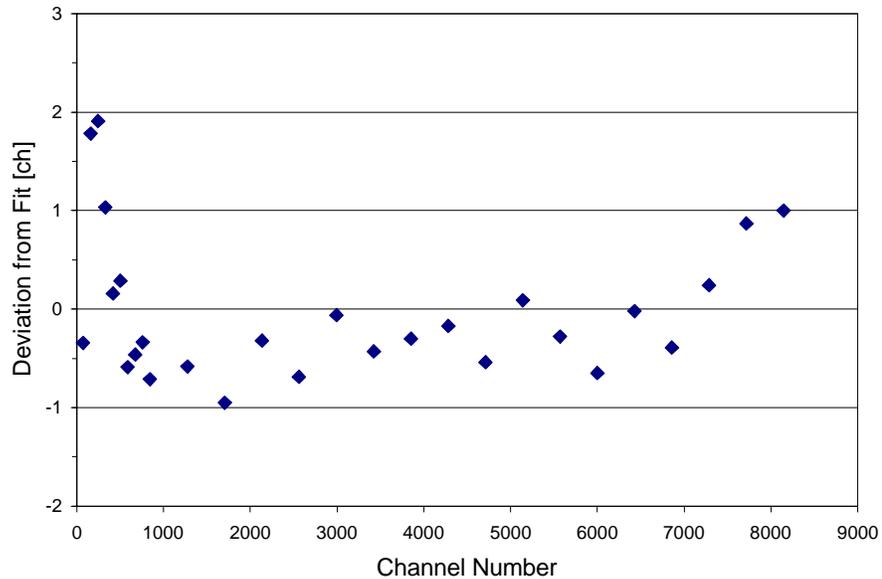
Plotting the deviations of the measured points from the fit yields:



The linearity of an ADC can depend on the input pulse shape and duration, due to bandwidth limitations in the circuitry.

The differential non-linearity shown above was measured with a 400 ns wide input pulse.

Increasing the pulse width to 3  $\mu$ s improved the result significantly:



#### 4. Conversion Time

During the acquisition of a signal the system cannot accept a subsequent signal (“dead time”)

Dead Time =

- signal acquisition time → time-to-peak + const.
- + conversion time → can depend on pulse height
- + readout time to memory → depends on speed of data transmission and buffer memory access - can be large in computer-based systems

Dead time affects measurements of yields or reaction cross-sections. Unless the event rate  $\ll 1/(\text{dead time})$ , it is necessary to measure the dead time, e.g. with a reference pulser fed simultaneously into the spectrum.

The total number of reference pulses issued during the measurement is determined by a scaler and compared with the number of pulses recorded in the spectrum.

Does a pulse-height dependent dead time mean that the correction is a function of pulse height?

Usually not. If events in different part of the spectrum are not correlated in time, i.e. random, they are all subject to the same average dead time (although this average will depend on the spectral distribution).

- Caution with correlated events!  
Example: Decay chains, where lifetime is  $<$  dead time.  
The daughter decay will systematically be lost.

## 5. Count Rate Effects

Problems are usually due to internal baseline shifts with event rate or undershoots following a pulse.

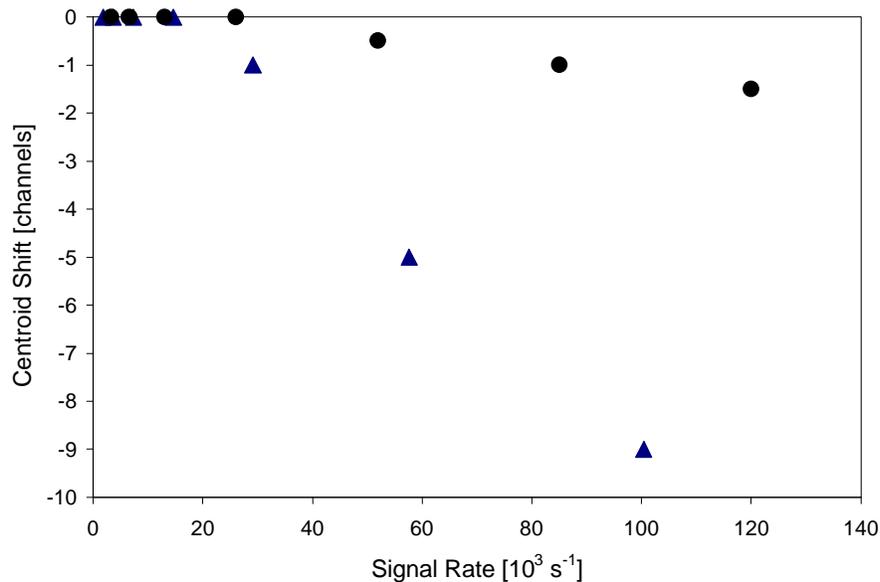
If signals occur at constant intervals, the effect of an undershoot will always be the same.

However, in a random sequence of pulses, the effect will vary from pulse to pulse.

⇒ spectral broadening

Baseline shifts tend to manifest themselves as a systematic shift in centroid position with event rate.

Centroid shifts for two 13 bit ADCs vs. random rate:



## 6. Stability

Stability vs. temperature is usually adequate with modern electronics in a laboratory environment.

- Note that temperature changes within a module are typically much smaller than ambient.

However: Highly precise or long-term measurements require spectrum stabilization to compensate for changes in gain and baseline of the overall system.

Technique: Using precision pulsers place a reference peak at both the low and high end of the spectrum.

(Pk. Pos. 2) – (Pk. Pos. 1) → Gain, ... then

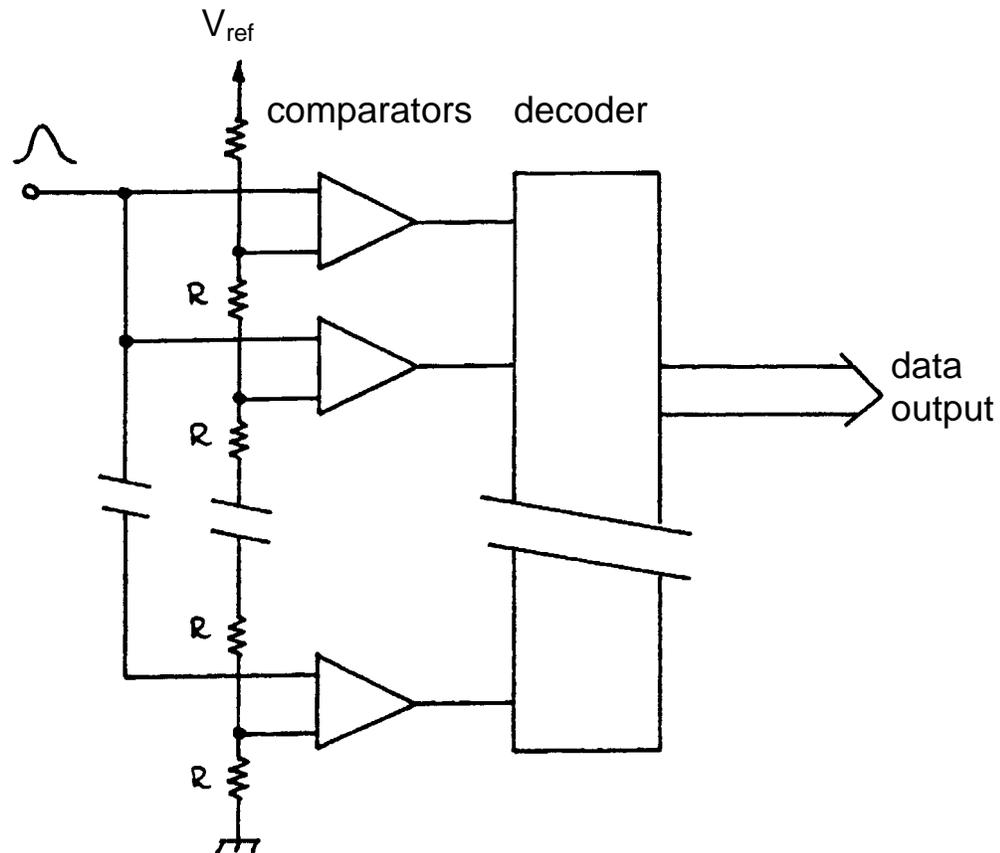
(Pk. Pos. 1) or (Pk. Pos. 2) → Offset

Traditional Implementation: Hardware,  
spectrum stabilizer module

Today, it is more convenient to determine the corrections in software. These can be applied to calibration corrections or used to derive an electrical signal that is applied to the hardware (simplest and best in the ADC).

# Analog to Digital Conversion Techniques

## 1. Flash ADC



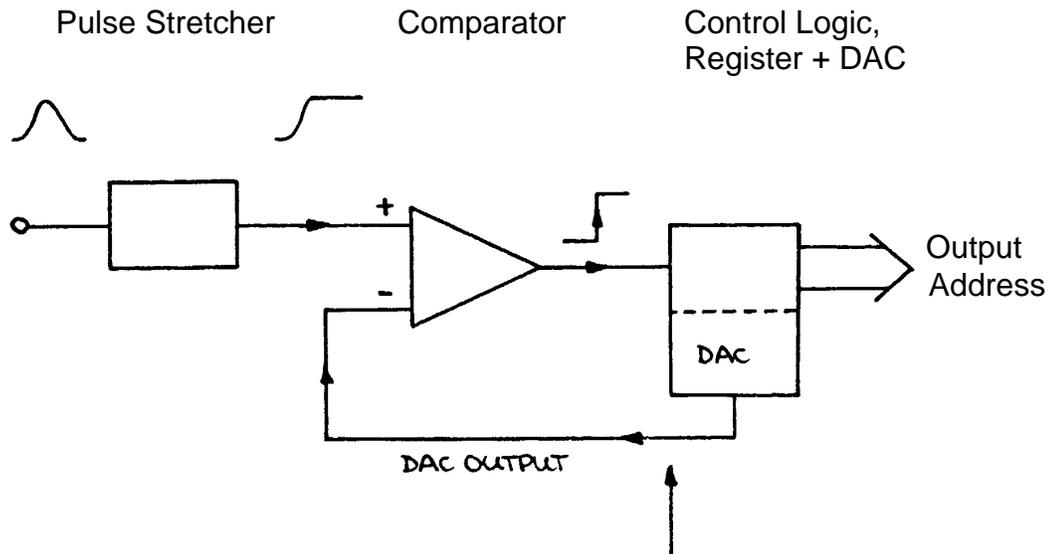
The input signal is applied to  $n$  comparators in parallel. The switching thresholds are set by a resistor chain, such that the voltage difference between individual taps is equal to the desired measurement resolution.

$2^n$  comparators for  $n$  bits (8 bit resolution requires 256 comparators)

Feasible in monolithic ICs since the absolute value of the resistors in the reference divider chain is not critical, only the relative matching.

Advantage: short conversion time (<10 ns available)  
Drawbacks: limited accuracy (many comparators)  
power consumption  
Differential non-linearity  $\sim 1\%$   
High input capacitance (speed is often limited by the analog driver feeding the input)

## 2. Successive Approximation ADC



Sequentially add levels proportional to  $2^n, 2^{n-1}, \dots, 2^0$  and set corresponding bit if the comparator output is high (DAC output < pulse height)

n conversion steps yield  $2^n$  channels,  
i.e. 8K channels require 13 steps

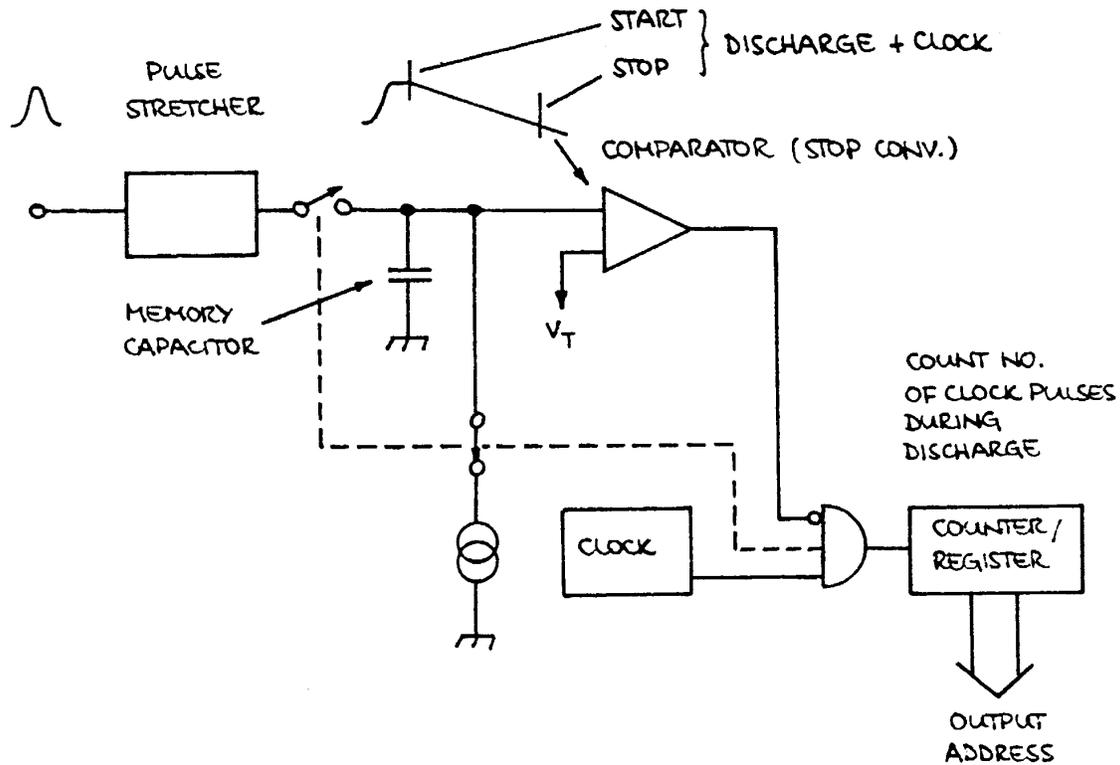
Advantages: speed ( $\sim \mu\text{s}$ )  
high resolution  
ICs (monolithic + hybrid) available

Drawback: Differential non-linearity (typ. 10 – 20%)

Reason: Resistors that set DAC output must be extremely accurate.

For DNL < 1% the resistor determining the  $2^{12}$  level in an 8K ADC must be accurate to  $< 2.4 \cdot 10^{-6}$ .

### 3. Wilkinson ADC



The peak signal amplitude is acquired by a pulse stretcher and transferred to a memory capacitor. Then, simultaneously,

1. the capacitor is disconnected from the stretcher,
2. a current source is switched to linearly discharge the capacitor,
3. a counter is enabled to determine the number of clock pulses until the voltage on the capacitor reaches the baseline.

Advantage: excellent differential linearity  
(continuous conversion process)

Drawbacks: slow – conversion time =  $n \cdot T_{clock}$   
( $n$  = channel number  $\propto$  pulse height)

$$T_{clock} = 10 \text{ ns} \rightarrow T_{conv} = 82 \mu\text{s} \text{ for 13 bits}$$

Clock frequencies of 100 MHz typical, but  
>400 MHz possible with excellent performance

“Standard” technique for high-resolution spectroscopy.

# Hybrid Analog-to-Digital Converters

Conversion techniques can be combined to obtain high resolution and short conversion time.

## 1. Flash + Successive Approximation or Flash + Wilkinson (Ramp Run-Down)

Utilize fast flash ADC for coarse conversion  
(e.g. 8 out of 13 bits)

Successive approximation or Wilkinson converter to provide fine resolution. Limited range, so short conversion time:

256 ch with 100 MHz clock  $\Rightarrow$  2.6  $\mu$ s

Results: 13 bit conversion in  $< 4 \mu$ s  
with excellent integral and differential linearity

## 2. Flash ADCs with Sub-Ranging

Not all applications require constant absolute resolution over the full range. Sometimes only *relative* resolution must be maintained, especially in systems with a very large dynamic range.

Precision binary divider at input to determine coarse range + fast flash ADC for fine digitization.

Example: Fast digitizer that fits in phototube base.  
Designed at FNAL.

17 to 18 bit dynamic range  
Digital floating point output  
(4 bit exponent, 8+1 bit mantissa)  
16 ns conversion time